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NASA-AMES HYBRID COMPUTER FACILITIES AND THEIR APPLICATION TO PROBLEMS IN AERONAUTICS

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INTRODUCTION

It has been our privilege at the Ames Research Center to be able to participate in the design and development of two advanced hybrid computing machines, the Ames Linkage System and the Digital Logic Simulator.

The Ames Linkage System was built around requirements of a specific simulation, and because of the magnitude of the mission, the unit was designed primarily to fit these specifications. The unusual features of the linkage are emphasized along with a general discussion of its capabilities.

The Digital Logic Simulator was developed for aiding in the expeditious solution of simulation problems containing logic elements. However, a wide variety of interesting applications of this device have been worked out at the Center and it is felt that these applications indicate the future potentialities of this class of machine. Three recent applications will be discussed in some detail.

The Ames Linkage System

When approaching the problem of simulating reentry vehicles over typical flight profiles in the earths atmosphere, the inadequacies of the analog computer for computation of the various navigation parameters become very troublesome. If one further contemplates space navigation simulation, the analog mechanization is totally inadequate. For these reasons Ames Research Center undertook to provide a link between the very extensive analog facilities and a modern digital facility to provide a combined

computational facility that could satisfactorily reproduce the flight characteristics of space vehicles.

Several major factors shaped the design of the linkage:

1) Physical separation of the analog and digital facilities,
2) Necessity for conservation of digital computer time for economic reasons,
3) Control and operation of the linkage invested in a remote simulation machine,
4) Extensive readout of digital computer values directly on simulator control panels.

Figure 1 shows graphically the physical separation of the two computer facilities. The analog computer, the linkage equipment, and simulation machine are located in the building in the upper right hand portion of the figure and the digital facilities in the building at the lower left hand portion of the figure. The white line shows the 2500 ft. path of the underground conduit that contains the 73 coax transmission lines that make the signal connections between the two computers. Digital signal transmission appeared the most desirable method of communication from the outset, but whether transmission of satisfactory digital wave shapes over this distance could be achieved was of paramount importance to the system design. The 73 lines permit parallel 16 bit plus sign data word and parallel 10 bit sense word communication in both directions simultaneously. While this system concept required more wire lines, it greatly simplified the final linkage hardware. Serial transmission was considered, but the data rates and equipment complications eliminated this mode of operation. From an

economic viewpoint, it makes very little difference if one or 100 transmission lines are used since serial transmission requires additional logic, higher speed logic, and more engineering design time than parallel transmission. The cables lie in salt water through much of the year, therefore, RG 62 A/U cable was used -- each line being 2500 ft. long so that no intermediate connectors are required.

Figure 2 shows the results of a test, run by Packard Bell Computer Corporation, to show the electrical performance of the final transmission system. The transmission system, which senses the current mode of the line, requires transmission line drivers between the input stage and the line. Line receivers and pulse shapers are required between the output of the line and the output stage for successful operation. Figure 2 shows the distortions of the actual transmitted signals and corrections effected by pulse reshapers in the transmission line receiver units. The 5 μsec. of delay shown by the oscillogram is introduced by the line length and the velocity of propagation characteristics of the transmission cable. Operational experience with this digital transmission link has been very satisfactory, with millions of words having been transmitted error free in both directions.

To permit a computer to stand idle is viewed as a felonious offense in a high pressure digital computer laboratory. Therefore, the introduction of a linkage system to connect on a flight simulator with its myriads of people, problems, and delays is viewed with some justifiable apprehension by those responsible for effective utilization of the digital equipment. Therefore, a

considerable effort has been expended to develop a method of efficiently interrupting the normal digital computer operations for flight simulation computations on a demand basis.

A Data Acceptance Routine (DAR) has been implemented and is shown in flow diagram form in Figure 3. The major points of the routine are:

1) Routine permanently stored in computer core,
2) Routine permits inputing of data from simulation with only a momentary halting of digital computer.
3) Routine permits efficient interlacing of production work with simulation work, with simulation given priority.

The object of the routine is to keep the digital in production operation until the moment a flight simulation begins. Similarly, at the termination of a simulation run, the digital equipment is rapidly returned to production work. The maximum changeover time is of the order of 10 seconds.

The major point of interest in the data acceptance routine is that data can be transmitted to the simulation program without dumping the production program. The key to this procedure is the fact that the digital computer can perform all the operations of the DAR, including testing for a compute code without disturbing ~~the~~ its arithmetic register.

The conversion components of the linkage such as the multiplexer (MPX), analog to digital converter (ADC), and the digital-to-analog converter (DAC) are all standard items of the 15 KC, 13 bit plus sign bit class and do not need any explanation.[1,2,3] Figure 4 shows a simplified block diagram of the signal paths between the digital and analog portions using the conversion components. The sense output lines of the digital machine direct

the channel selection of the DAC and ADC units permitting random selection of the ADC and DAC channels.

Figure 5 is a photograph of the pilots control panel of the reentry vehicle being simulated. Of principal concern here are the computer display panel (upper right) and the keyboard panel. The control panel permits operational control of the entire linkage-computer system. The flow of data to the digital computer from both analog and pilot inputs is shown diagrammatically in Figure 6. In addition to digitized data from the ADC, the vehicle pilot has the ability to input digital information through the keyboard panel via the digital input data lines. The function of the check display on the computer display panel is to give the pilot a visual indication of his manual data input. Operational instructions are entered into the system by the large pushbuttons on the keyboard panel via the sense input lines.

The data flow from the digital computer is illustrated in Figure 7. The sense output codes address the control panel selector on the ADC-DAC channel selector. This determines whether the information from the data output lines are transmitted to the displays or to the DAC units. Figures 6 and 7 illustrate the extensive digital communication link between the simulator and the digital computer. The most potent use for this display capability is during space flight portion of the mission simulation. Here also maximum advantage of the Data Acceptance Routine can be seen, for during midcourse phases only occassional use of the simulation computer is needed for the navigational phase of a space flight. Call up times of only several seconds per 15 minute intervals are required during midcourse navigation.

The reentry phase requirements on combined computer systems are substantially different from those of midcourse phase. Primarily, this occurs because aerodynamics of the vehicle are added to the particle dynamics of the midcourse phase. From the computer viewpoint, continuous operation of both the digital and analog portions are required, with heavy dependance on the analog for short period modes of the simulation. While a detailed discussion of the reentry mechanization is beyond the scope of this paper, a brief discussion is of interest. The entire reentry mission is approximately of 15 minutes duration and the digital computer must be on line continuously. For this reason, many of the advantages of the DAR are not used, particularly the inputing of data while doing production work. Therefore, only the exit portion of the DAR is used in the reentry phase.

Figure 8 is a flow diagram of the computer operation for the reentry phase. The simulation program is loaded into the digital computer as standard production program. The simulation operator actuates the I.C. pushbutton and the digital sends the I.C. values to the analog and goes, automatically, off line. After the check-out of the simulator is completed, the simulation must be re-instated, by production methods, into the digital computer. The operate cycle then commences as shown on the chart. This continues until either the I.C. or Halt pushbuttons are actuated which automatically exits the digital computer.

The system of equations employed in this reentry phase are those devised by Forgarty and Howe of the University of Michigan.[4] This system, called the Modified Flight Path Axis System, introduces several special axis frames, two of which need explanation for this discussion. These two frames are called the E frame and H frame.

The origin of the E-frame is at the center of gravity of the vehicle; the vector components point north, east and down. The H-frame differs from the E-frame by the heading angle of the vehicle velocity vector. The analog computer receives the standard pilot inputs, calculates the aerodynamic and jet reaction forces in the Body Axis frame, and transforms these forces into the E-frame. The E-frame forces are then digitized and serve as inputs to the digital computer. The digital then transforms the E-frame forces into the H-frame forces; calculates the H-frame velocities and the E-frame velocities; calculates the latitude, longitude and altitude of the vehicle; and calculates dynamic pressure and mach number. The E-frame velocities, the vehicle position, the dynamic pressure and the mach number serve as outputs from the digital computer to the analog computer. The analog computer computes the standard body axis rotational equations, the conventional Euler angles, and the direction cosines.[5] Each computational cycle requires approximately 125 μsec. with the digital computer programmed in fortran and using a parabolic integration routine to integrate the forces and velocities.

7/12

THIS IS QUESTIONED
IS IT 125 millisec OR 125 μs.
— 125 μs APPEARS FAST FOR THE TYPE OF MACHINE & COMPUTATION INVOLVED
H Lowell

The Ames Digital Logic Simulator (DLS) was placed in operation during September 1962. Since that time it has received considerable attention from prospective users of similar equipments as to the usefulness of logical computing elements in an analog simulation laboratory.

The original impetus for the DLS was a simulation requirement for aid in studying an earth orbit satellite called O.G.O. (Orbiting Geophysical Observatory). It was most troublesome to provide proper simulation of the reaction-jet controllers and the logical autopilot system with standard analog components. For instance the analog mechanization of the O.G.O. logic controllers took some 400 diodes, 135 amplifiers, and two specially fitted EAI 31R patch panels. The spectre of having to repeat this process resulted in a contract award to Electronics Associates to develop the DLS, known commercially today as the EAI DOS 350.

The DLS was designed to be an accessory to the analog simulation computers. It was, therefore, equipped to easily connect into and function with standard real time analog computers. As presently constituted the computer has the logical and digital components shown in Figures 10A and 11B. All these components are available for interconnection through a removable problem pre-patch panel and all connections are made by the familiar analog patching method.

For purposes of illustration, the computer components have been divided into two general categories:

1) logical operation components,

2) digital word components.

The logical units permit mechanization of Boolean algebra functions, and their insertion into analog computer loops is accomplished by comparators and D/A switches. Comparators serve to introduce analog events into the logic computer, the state change of their digital output marking the coincidence of analog computer variables. The digitally-controlled analog switches, or D/A switches, permit the introduction of logical events into control loops of the analog program by controlling the inputs to operational amplifiers. The basic logic elements of the DLS, shown in Figure 10, are self-explanatory. The pre-organized logic elements shown in the same figure are elements that would require sizeable sections of basic logic to mechanize. Therefore, basic logic is prepackaged to perform these more difficult functions by simple input and output connections. This greatly simplifies the programming, better utilizes the available patch panel holes and increases the cost.

The digital word components illustrated in Fig. 11 consist of the usual multiplexer (MPX), analog-to-digital converter (ADC) and digital-to-analog converter (DAC) units similar to those readily available on the commercial market. These units provide the capability of translating analog values into digital numbers and vice versa. The digital numbers so generated can be stored, outputed or otherwise operated on by use of the storage and readout elements shown in Figure 11. The memory elements (SM8, etc.) are acoustic delay lines cut to various multiples of the 16 bit digital words used in the DLS. The memory buffer (MB) is an element for temporary holding of digital words for insertion into memory lines at the appropriate interval. The paper tape punch and reader permit

fast input and output of DLS logic states or digital numbers.

The DLS has been applied to a variety of problems at the Ames Research Center and promise for future applications seems unlimited. Particularly gratifying has been the new areas of problem work available to the simulation computers when interconnected with the DLS. These areas include:

1) Data applications
   a. Data reduction
   b. Data work-up
   c. Data readout

2) Simulation Applications
   a. Simulation of logical control systems
   b. Simulation of transport delays
   c. Simulation display generation

3) Computer Control Applications
   a. Analog computer control
   b. Linkage system control

To illustrate the future potential and present success of this machine, several problems that have been run will be discussed.

Figure 12 illustrates a method of computing average heart rate from electrocardiograph (ECG) signals that have been stored on magnetic tape. The actual problem required the reduction of continuous ECG data from two subjects enclosed in a small capsule for seven days. If one assumes one heart beat per second, the data tapes contained 1.8 million heart beats of the two subjects.

The requirements of the biotechnology department was a time average of heart rate over a five (5) minute period; this to be computed continuously for the seven (7) days accumulation of test data. Figure 12 shows the basic program to compute heart rate from this ECG data. A comparator detects the peaks by setting the reference level to intersect the main peak only. The output of the comparator is accumulated in counter for five minutes then the contents of counter are printed out, the counter cleared and begins counting again. However, playback in real time is very uneconomical, and playback at 16 inches per second (IPS) was selected. The box of Figure B shows the relative record to playback timing obtained by simply increasing the playback tape speeds. The tape playback of 16 IPS from a recording speed of 1 7/8 IPS lowers the running time of the playback computation to 10.5 hrs. The logic components and comparators present no difficulty at this speed, as they still are orders of magnitude faster than playback events (i.e., comparators switch in 10μsec.). Of concern at this playback rate is the speed of the printout mechanism, which at this time was an HP560 printer. This problem is handled by devoting one register as a holding and printout register while another register accumulates the immediately following counts. For two subjects the printer is permitted nine (9) seconds per printout; a very satisfactory safety margin for standard printers such as the H-P (60).

The method of Figure 12 has the disadvantage of readily responding to noise spikes and secondary heart actions such as systoles. To aid in discriminating against these extraneous signals, a "window" generator shown in Figure 13 was mechanized

using a differentiator, two flip-flops and a down-counter. Figure 14 illustrates the final circuit configuration. Using timing marks from the data, instead of from machine-generated timing, the system can be operated at any tape speed, provided the "window" is adjusted to fit the playback pulse interval. Scaling of the output readings for direct printout of average heart rate is acccomplished by the double counting effect of the leading edge-trailing edge-differentiator action and division by 10 on the BCD counter by shifting the decimal point, resulting in the required division by five (5). A summary of necessary logic elements shows:

19 flip-flops

90 AND gates

15 decades down-counting

8 decades up-counting

8 decades down-counting (used as holding registers).

Total running time, including tape handling, was two days.

A somewhat allied technique of processing data by level selection and accumulation of resultant counts has been exploited by Mr. W.D. Cameron of the Ames Research Center staff, which has been reported separately in detail.[6]

An example of the versitility of the DLS in flight simulation problems was particularly apparent in its application to a tracking task simulator shown in Fig 15. In this investigation, the statistics of tracking errors of pilots with randomly variable initial rotational accelerations of the vehicle were under study. Figure 15 shows the degree of participation of the DLS in the simulation. The DLS:

1) Controls analog computer under pilot command,

2) Generates control pulses for insertion into analog computed dynamics,

3) Accumulates control pulses for fuel consumption computation,

4) Randomly selects +, - zero reference independently for three (3) integrator IC potentiometers,

5) Generates the oscilloscope display pattern from analog computer outputs,

6) Records all data output channels on punched paper tape.

In the operation of the simulation, the pilot steers the display by using a standard bang-bang controller. Upon superposition of the target dots, the pilot actuates the "Read" switch, which is the basic control input to the DLS, and the following sequence then occurs:

1) DLS places analog in hold,

2) DLS reads out seven (7) end-point quantities by actuating the multiplexer, ADC, paper tape punch recording system,

3) DLS places analog in IC,

4) DLS sets three new IC conditions,

5) DLS waits 0.5 seconds for IC chargint time,

6) DLS places analog in operate and

   a. generates display to pilot

   b. generates control pulses

   c. accumulates control pulses.

Of particular interest in this problem was the employment of the high speed paper tape punch I/0 unit instead of the standard ADIOS typewriter readout. The readout of seven (7) quantities on the ADIOS took a minimum of 21 seconds and the

addition of additional readout points was essentially limited by the slow ADIOS speed. Since hundreds of such runs are necessary, this waiting period amounts to hours of idle computer and pilot time. The DLS conversion and punch equipment was employed as shown in Figure 17. The converted values are transferred in character groups of four bits to the punch drivers in parallel. It takes 3 lines of punching to represent a 12 bit binary word and one line for the sign. A fifth (5) line is used for indexing. The maximum speed of the readout is, therefore, 22 binary words per second as the punch has a 110 character per second punching rate. The ADC, at 4,000 words/sec., is no limitation whatever to the output rate.

The time required for recording the necessary output data, placing new IC's on the analog, resetting and putting into operate is 0.8 seconds as compared to 21 seconds of the ADIOS -- a substantial improvement. In fact, for a human operated device like this it is too fast and some additional waiting time for human recovery has to be introduced. The interval of 0.8 seconds is just too short, being about long enough to push the read button and blink your eyes before a completely new run has begun.

After a series of runs are completed, the paper tapes are taken to the data processing laboratory for immediate processing and storage on magnetic tape. When sufficient runs for statistical evaluation are completed, the standard digital data processors can compute any desired functions or otherwise service the data. This method of data taking represents a major saving in technical manpower in running this type of program, and makes analog-computed results

instantly available to powerful digital computer analysis.

The DLS portion of the problem uses the following components:

42 Flip-flops
103 AND gates
30 D/A switches
6 GC up-counters
9 PC down-counters
3 Shift registers
7 Comparators
1 MPX, ADC, PTP
2 DAC

The results of this program have been most gratifying.

The primary purpose ~~for acquiring~~ the memory system in the DLS was for the simulation of transport delay. The first delay simulation has been implemented at the Center and some discussion of the preliminary experience using digital storage methods seems appropriate.

The basic problem involved the simulation of a jet engine control system at supersonic speeds, shown in Figure 18. The transport delays of the shock disturbances at the inlet to the exit were mechanized by using available DLS components of Figures 10 and 11. The required delays were, ~~as shown in Figure 6~~, 2.5, 1.67 and 0.714 seconds respectively. Available delay lines are 256 (SM8), 64(SM6) and 16(SM4) words long. Noting that sampling rate is the ratio of line length to delay required, the chart of Figure 19 shows the required sampling periods. These sampling frequencies are, unfortunately, unrelated harmonically and because there are three simultaneous delay channels in operation but only one ADC in the analog realm, data skewing results and accurate

sampling becomes very difficult to achieve even if a random access MPX and sample hold inputs were available. These latter components were not available so an alternate scheme of sampling in the digital realm was devised. Illustrated in Figure 19, the method uses the maximum up-dating rate of the MPX-ADC combination into three one-word memory buffers (MB). Each signal is sampled 1,300 times/second and the MB unit is constantly supplied with new data. The digital sampling for the delay of each channel is effected by ANDing a "sample" signal with the MB output. Simultaneous with inputing the delay line, the proper word must be transmitted to the waiting DAC. However, if the proper word is not in the output position, the transfer process must be held up until the memory circulates the desired word to the output position. This length of time varies depending on the memory access time. In the SM8, the access time is 2 milliseconds. This 2 milliseconds becomes the maximum holding time before the sampler can enter information into memory, but on the average will be substantially less than 2 milliseconds. Notice, though, the updating of MB continues so that when the appropriate transfer time does occur, later information has been put into the MB by the ADC, MPX combination. Also the effect is always to delay ~~the output word~~ it on the word in the line somewhat. It is believed that the errors introduced by these delays are small compared to other system inaccuracies such as the ADC, sampling, etc. However, problems of programming transport delays on digital equipment have been glossed over and considerable investigation is needed to find a maximum accuracy, minimum component program for multiple channel delays. Such efforts are under way at this Center.

Further, a substantial improvement in the programming methods for digital word components are required. At present, a great deal of effort is expended to decipher the manufacturers cryptic instruction manuals which are devoid of the most important item, a timing diagram. These problems are to be expected when stepping to a new area, and adjustments and experience can be expected to make later machines much more manageable in this respect.

CONCLUSION

Two major hybrid computer systems have been described briefly, emphasizing those features which make them extremely potent in the general field of research flight simulators.

The Ames Linkage System, while following the familiar "slender coupling"[5] design concept, has successfully connected two remote computers together in a simulation application. This, combined with extensive remote readout and control and the unique Data Acceptance Routine, makes elaborate space vehicle flight simulation possible at the Center. The use of the Linkage in the reentry phase has been discussed.

The Digital Logic Simulator on the other hand represents a new computer concept at this Center. The machine has found widespread use in simulation laboratory due basically to its general purpose design. The applications discussed have been selected to highlight the unique capabilities of this type of equipment in hybrid computation.

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3. Anon.: DA6 Digital-to-Analog Converter Technical Manual PBC 3003, Packard Bell Computer Company, 1905 Armacost Ave., Los Angeles 25, Calif. September 1, 1961

4. Fogarty, L.E., Howe, R.M.: Flight Simulation of Orbital and Reentry Vehicles, Part II - A Modified Flight Path Axis System for Solving the Six Degree-of-Freedom Flight Equations. ASD Technical Report 61-171 (II), October 1961

5. Ibid. p. 25

6. Cameron, W.D.: Determination of Probability Distributions Using Hybrid Computer Techniques. Proceeding of the International Symposium of Analog and Digital Techniques Applied to Aeronautics. September 9-12, 1963

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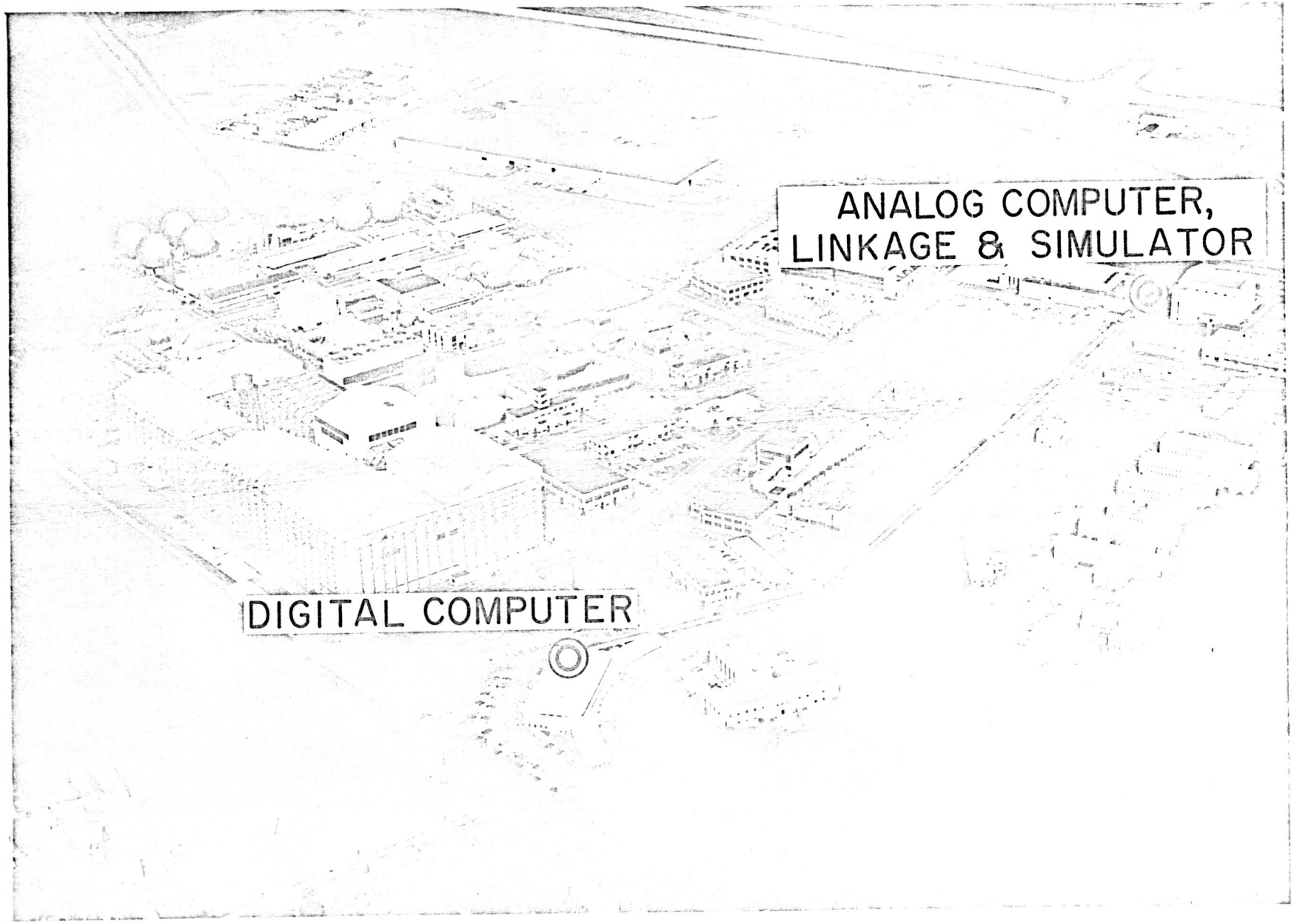

FIG 1

OSCILLOGRAPH OF 2500 FT TRANSMISSION

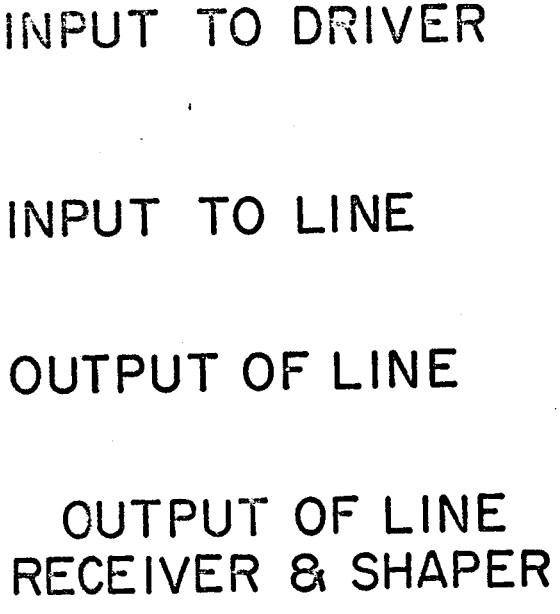

Fig 2

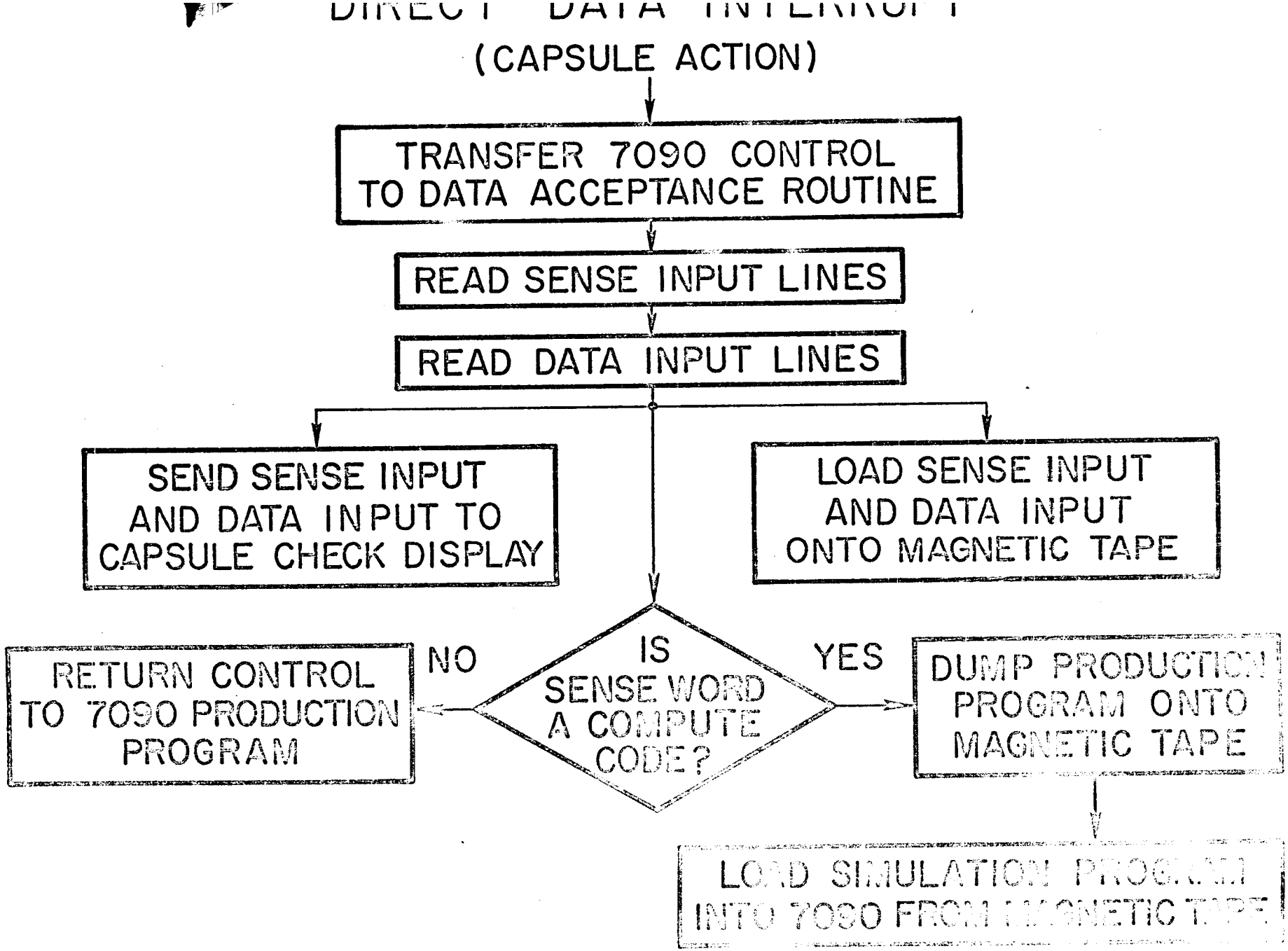
DIRECT DATA INTERRUPT
(CAPSULE ACTION)
TRANSFER 7090 CONTROL TO DATA ACCEPTANCE ROUTINE
READ SENSE INPUT LINES
READ DATA INPUT LINES
SEND SENSE INPUT AND DATA INPUT TO CAPSULE CHECK DISPLAY
LOAD SENSE INPUT AND DATA INPUT ONTO MAGNETIC TAPE
IS SENSE WORD A COMPUTE CODE?
NO
YES
RETURN CONTROL TO 7090 PRODUCTION PROGRAM
DUMP PRODUCTION PROGRAM ONTO MAGNETIC TAPE
LOAD SIMULATION PROGRAM INTO 7090 FROM MAGNETIC TAPE

Fig 3

SIGNAL LINKAGE BETWEEN ANALOG AND DIGITAL COMPUTERS

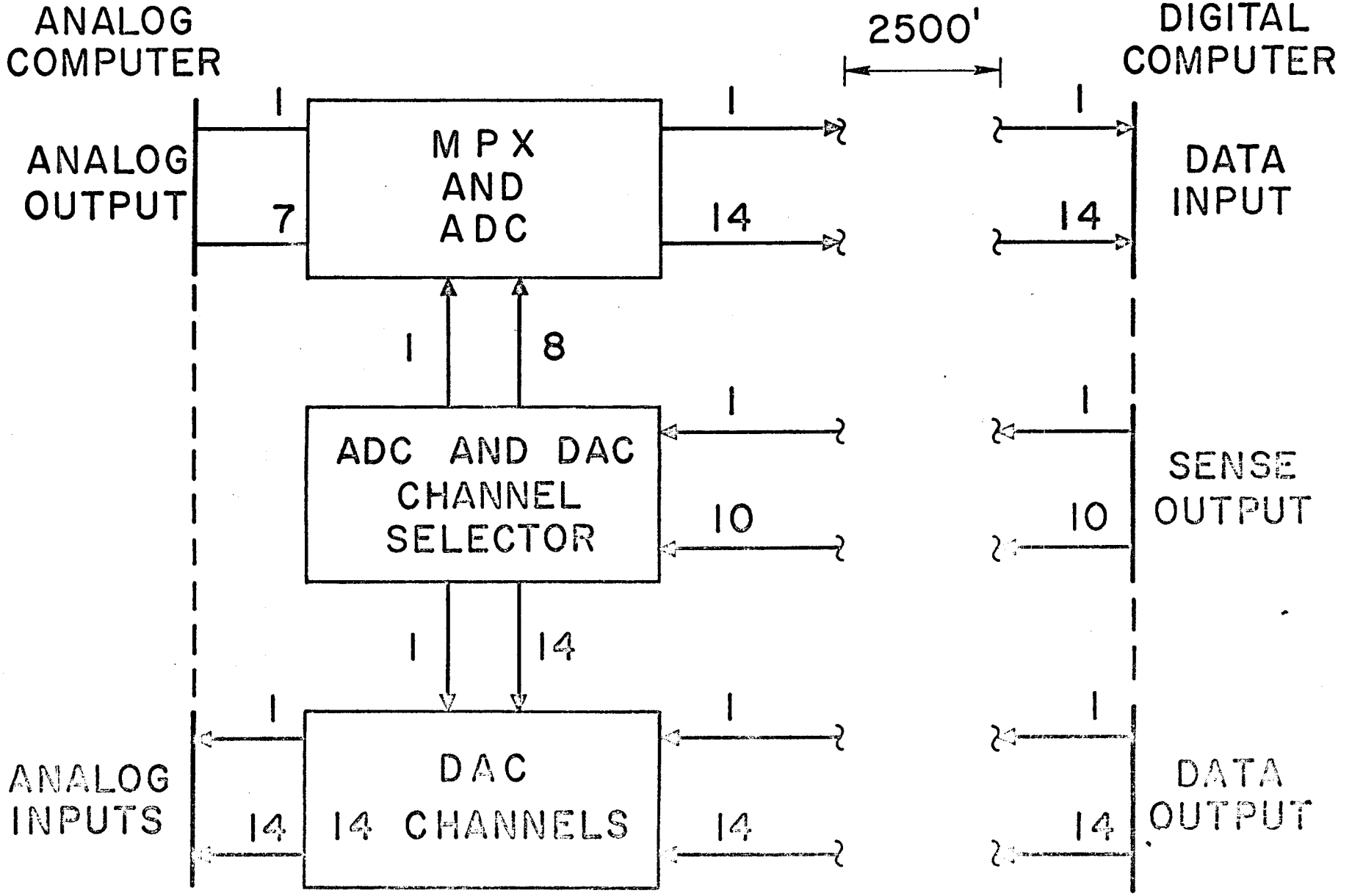

Fig 4

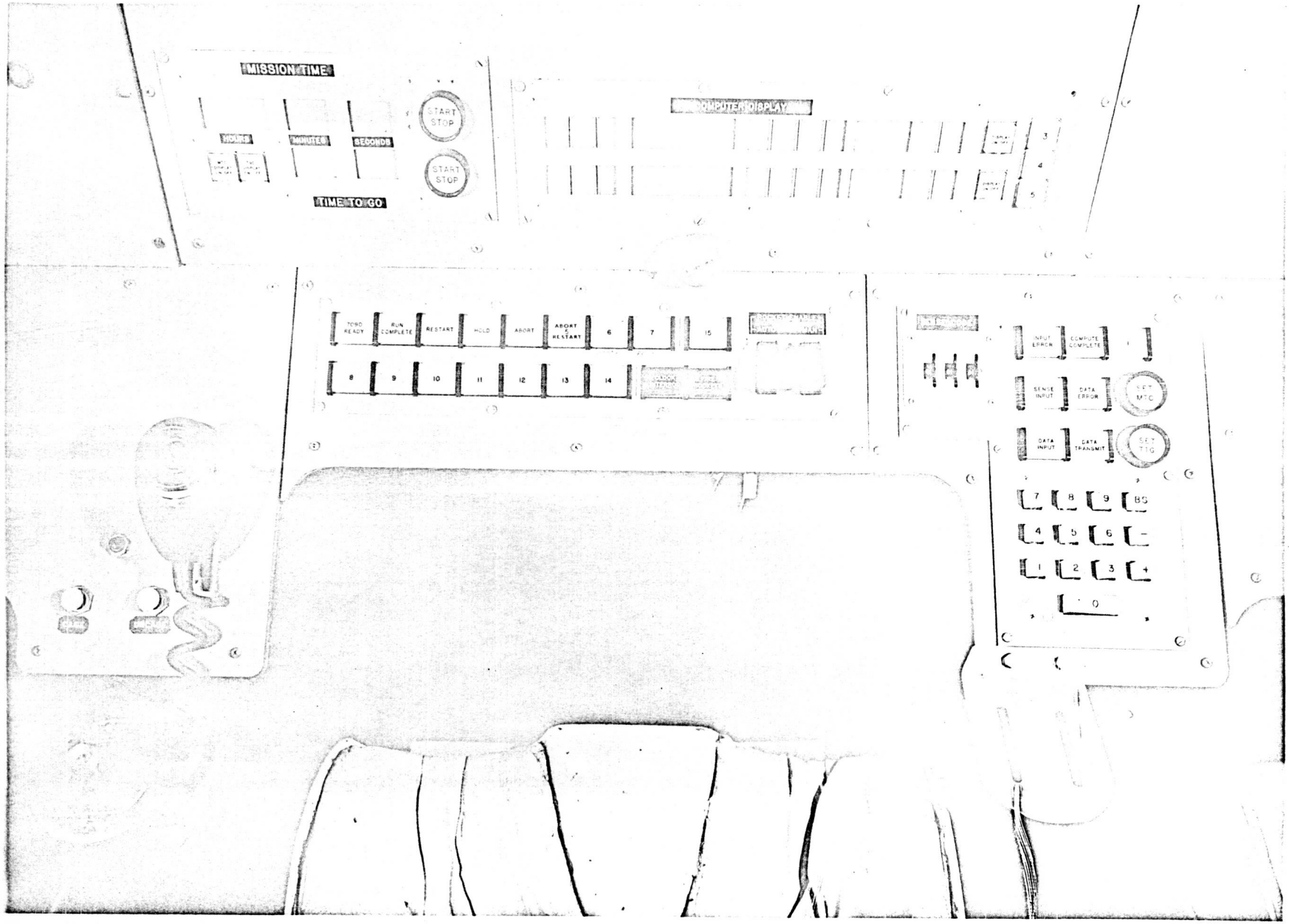
MISSION TIME
HOURS
MINUTES
SECONDS
START STOP
START STOP
TIME TO GO
COMPUTER DISPLAY
TOPO READY
RUN COMPLETE
RESTART
HOLD
ABORT
ABORT & RESTART
6
7
15
8
9
10
11
12
13
14
INPUT ERROR
COMPUTE COMPLETE
SENSE INPUT
DATA ERROR
DATA INPUT
DATA TRANSMIT
KEY MTC
KEY TRK
7
8
9
BS
4
5
6
-
1
2
3
+
0

FIG 5

INFORMATION FLOW FROM CAPSULE TO DIGITAL COMPUTER

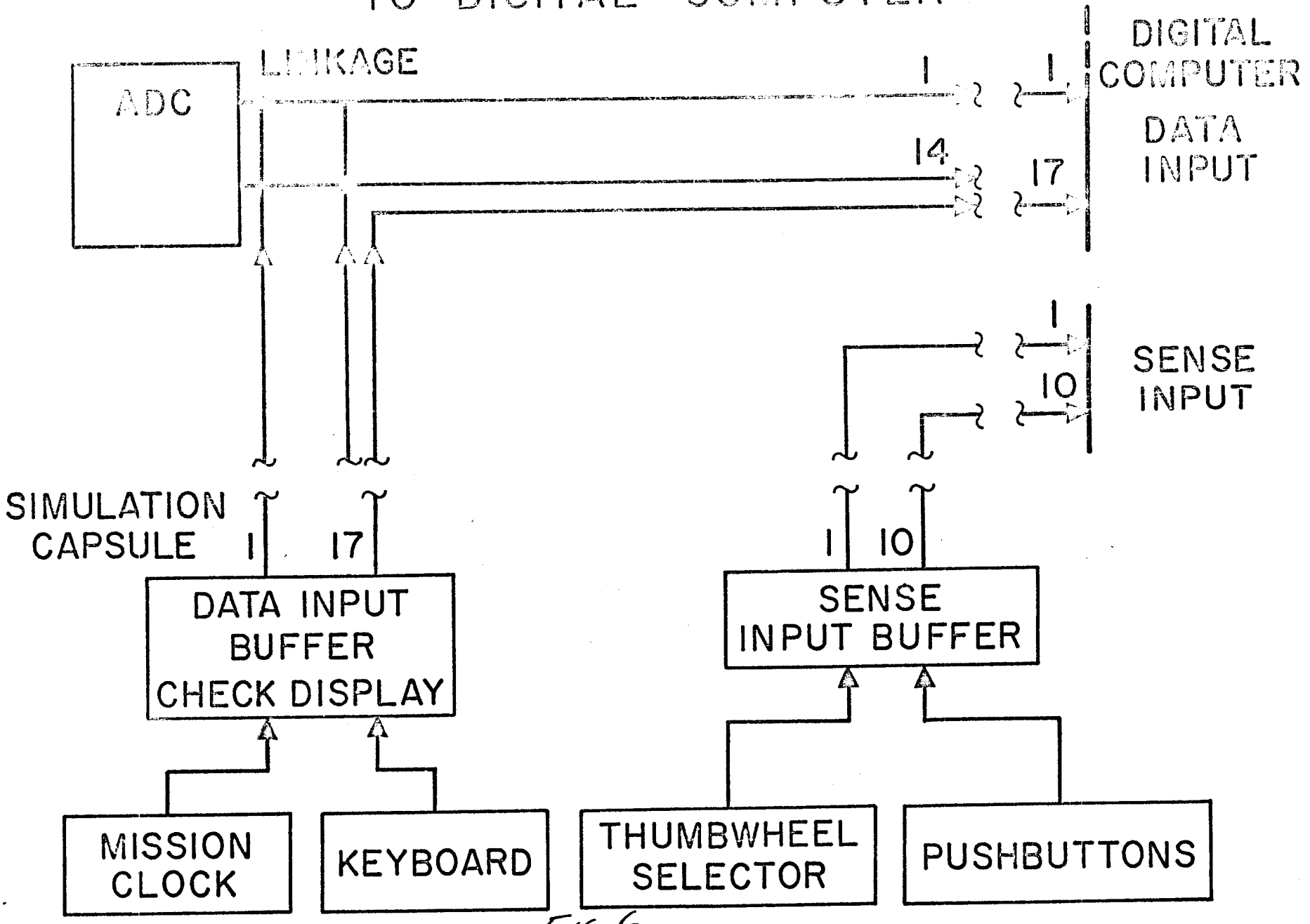

FIG 6

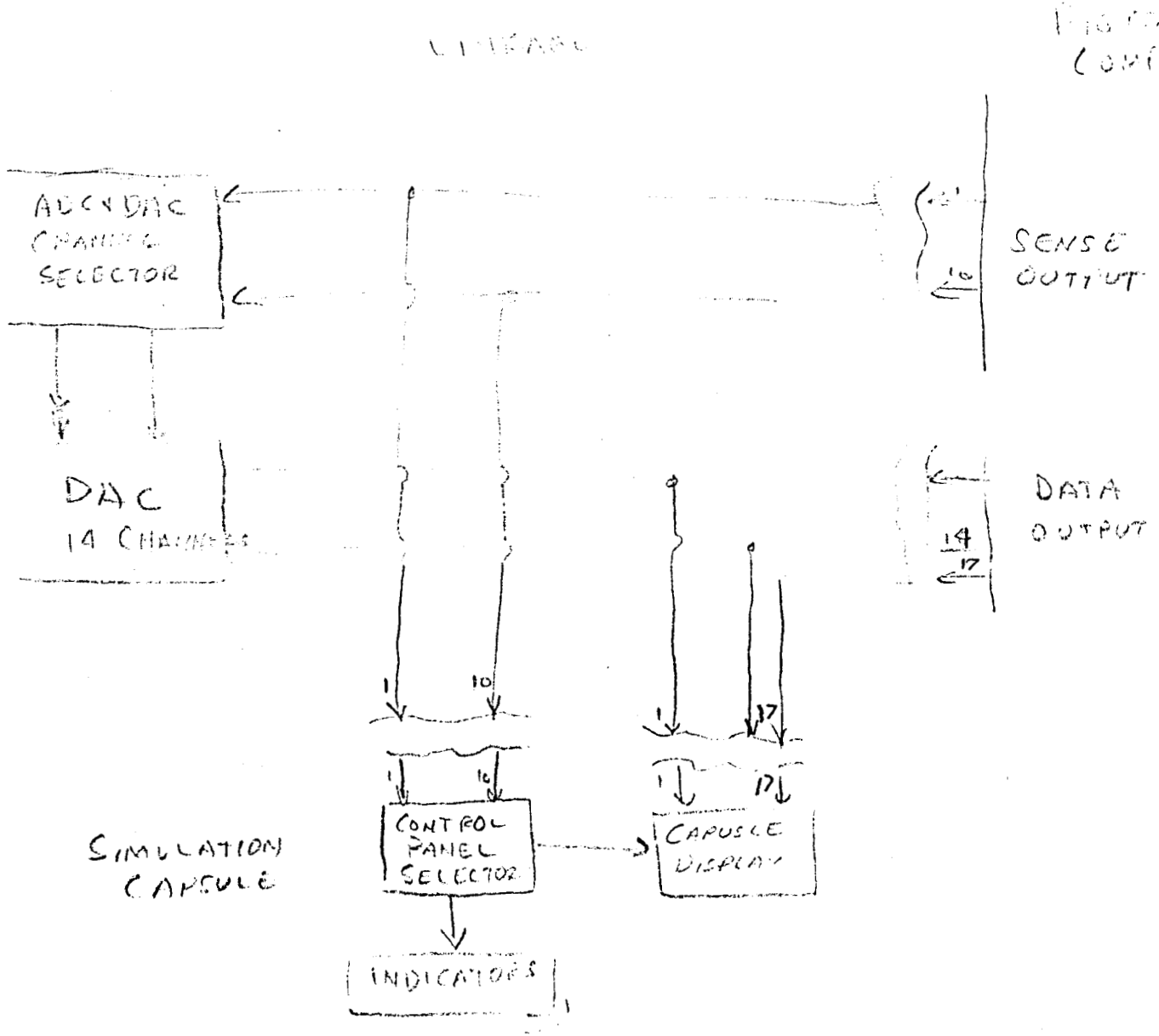

FIG 7) BLOCK DIAGRAM OF INFORMATION FLOW FROM DIGITAL COMPUTER TO CAPSULE

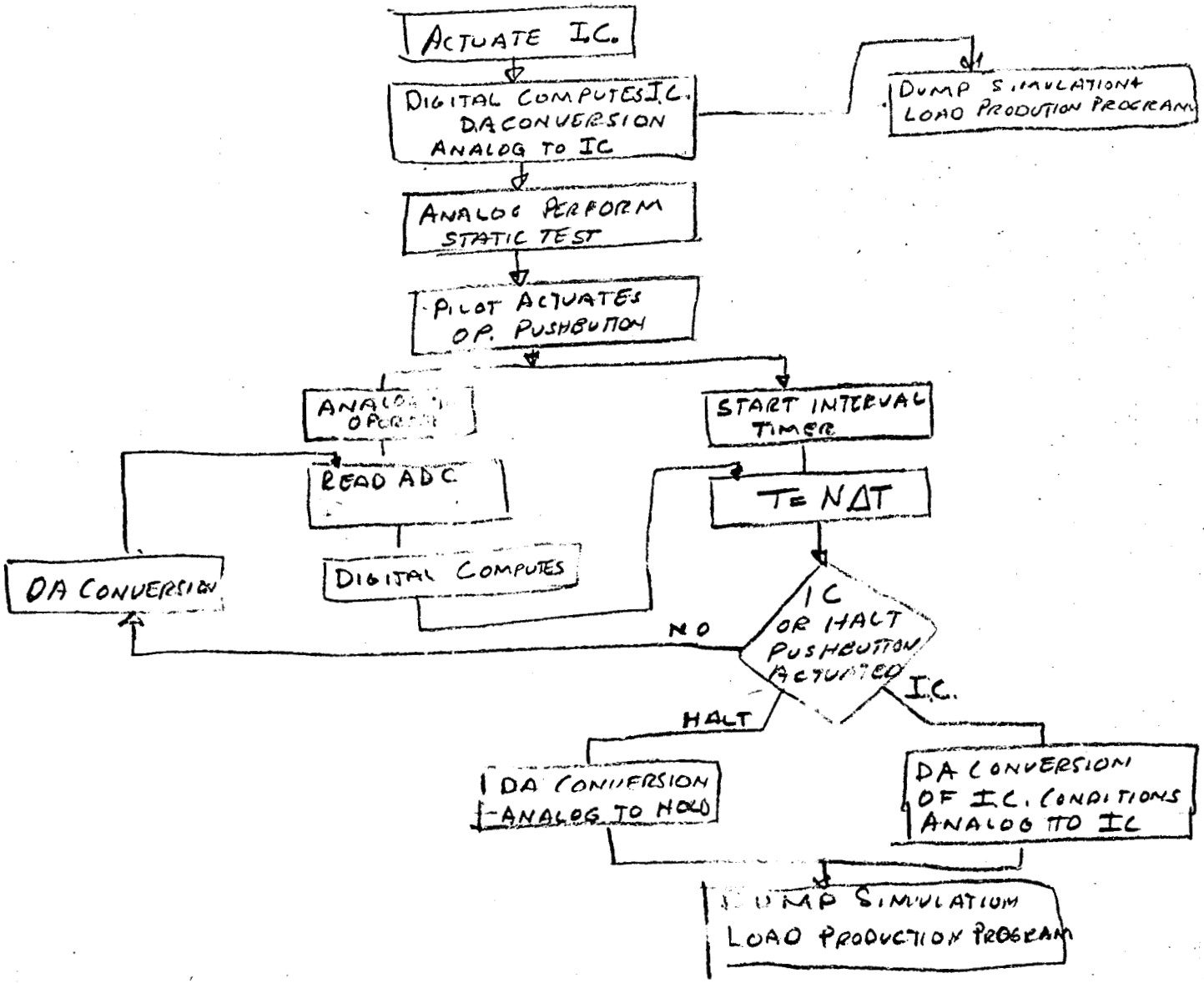

FIG8 FLOW DIAGRAM OF REENTRY PHASE PROGRAM

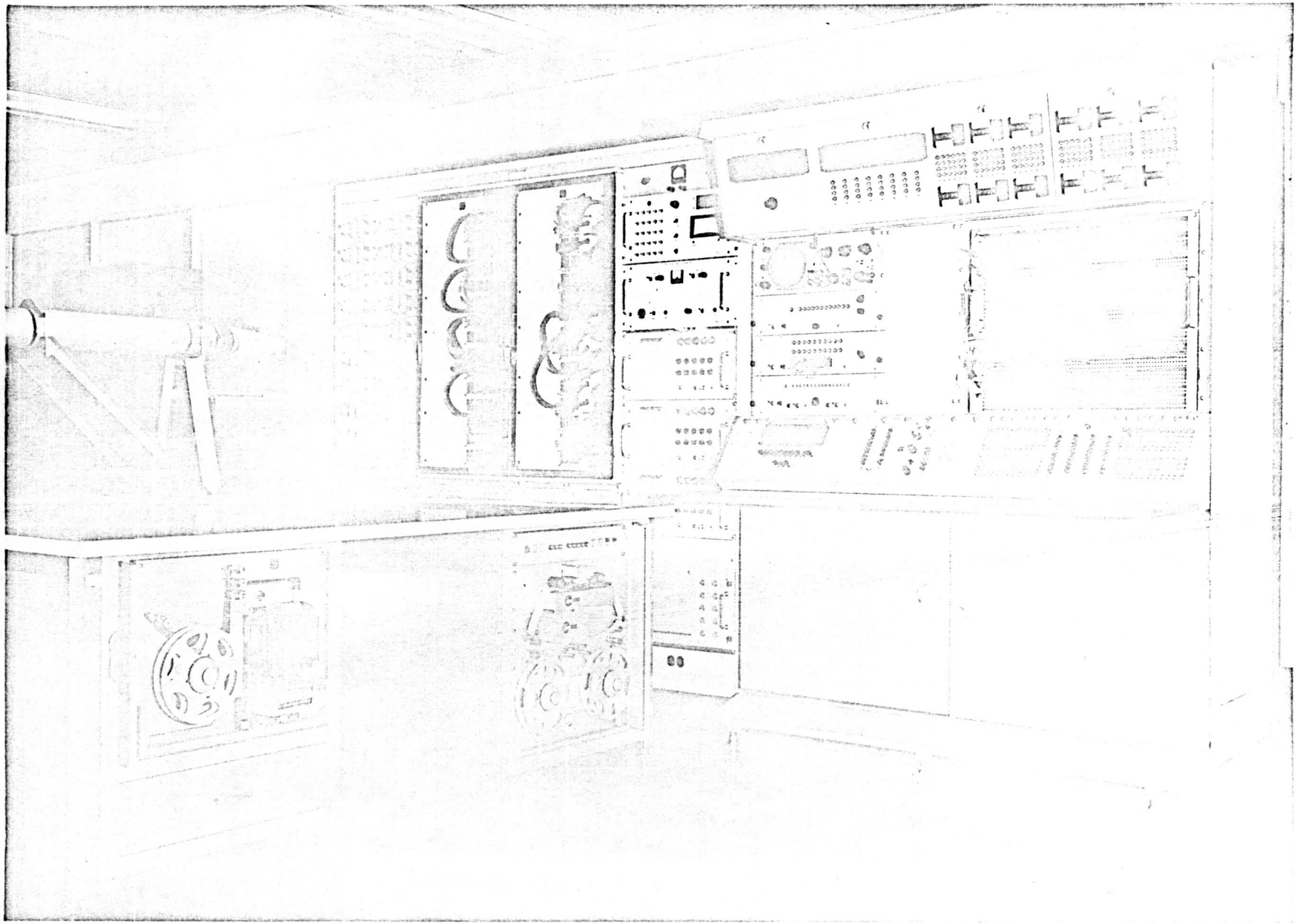

Fig 9 Ames DLS

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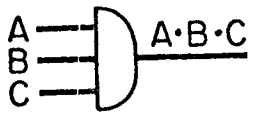
AMES RESEARCH CENTER, MOFFETT FIELD, CALIFORNIA

LOGICAL PROGRAMMING ELEMENTS AVAILABLE ON DIGITAL LOGICAL SIMULATOR



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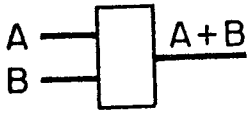

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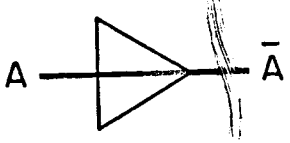
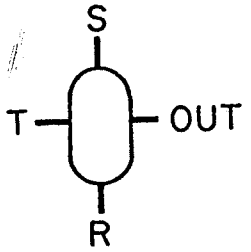
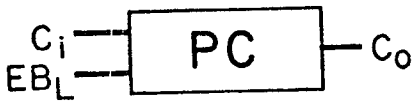


NOT



RST FLIP FLOP

BASIC LOGIC ELEMENTS



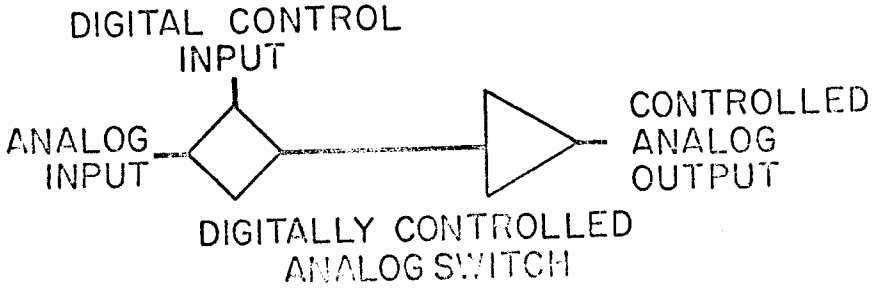
PRESETABLE BCD DOWN COUNTERS

GENERAL PURPOSE UP COUNTERS (BCD OR BINARY)

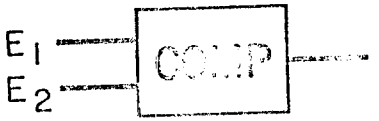
SHIFT REGISTERS

DIFFERENTIATORS

PREORGANIZED LOGIC ELEMENTS



DIGITALLY CONTROLLED ANALOG SWITCH

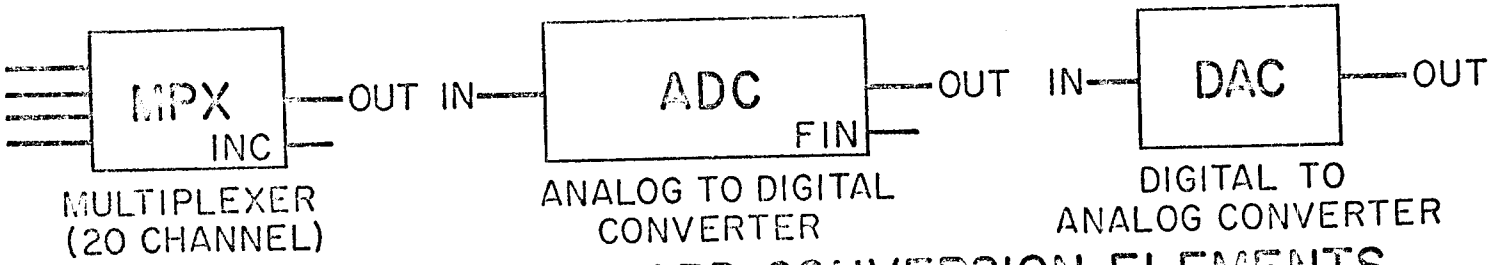


ANALOG COMPARATOR WITH DIGITAL OUTPUT

ANALOG-TO-LOGIC & LOGIC-TO-ANALOG ELEMENTS

Fig 10

LOGICAL PROGRAMMING ELEMENTS AVAILABLE ON DIGITAL LOGICAL SIMULATOR

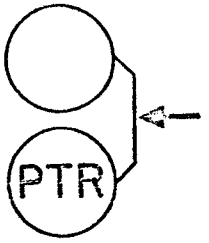


MULTIPLEXER (20 CHANNEL)

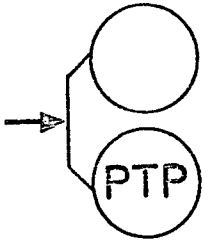
ANALOG TO DIGITAL CONVERTER

DIGITAL TO ANALOG CONVERTER

ANALOG TO DIGITAL WORD CONVERSION ELEMENTS



PAPER TAPE READER (500-1000 C/S)

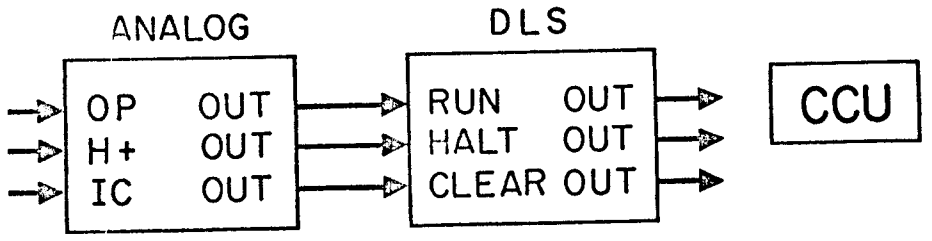


PAPER TAPE PUNCH (110 C/S)

DELAY LINE MEMORY (DIGITAL WORD STORAGE OF) (256,64,16 WORDS)

MEMORY BUFFER (1 WORD STORAGE)

INPUT/OUTPUT AND STORAGE ELEMENTS



MODE CONTROLS OF COMPUTERS

MEMORY CLOCK & WORD TIMER

VARIABLE FREQUENCY CLOCK

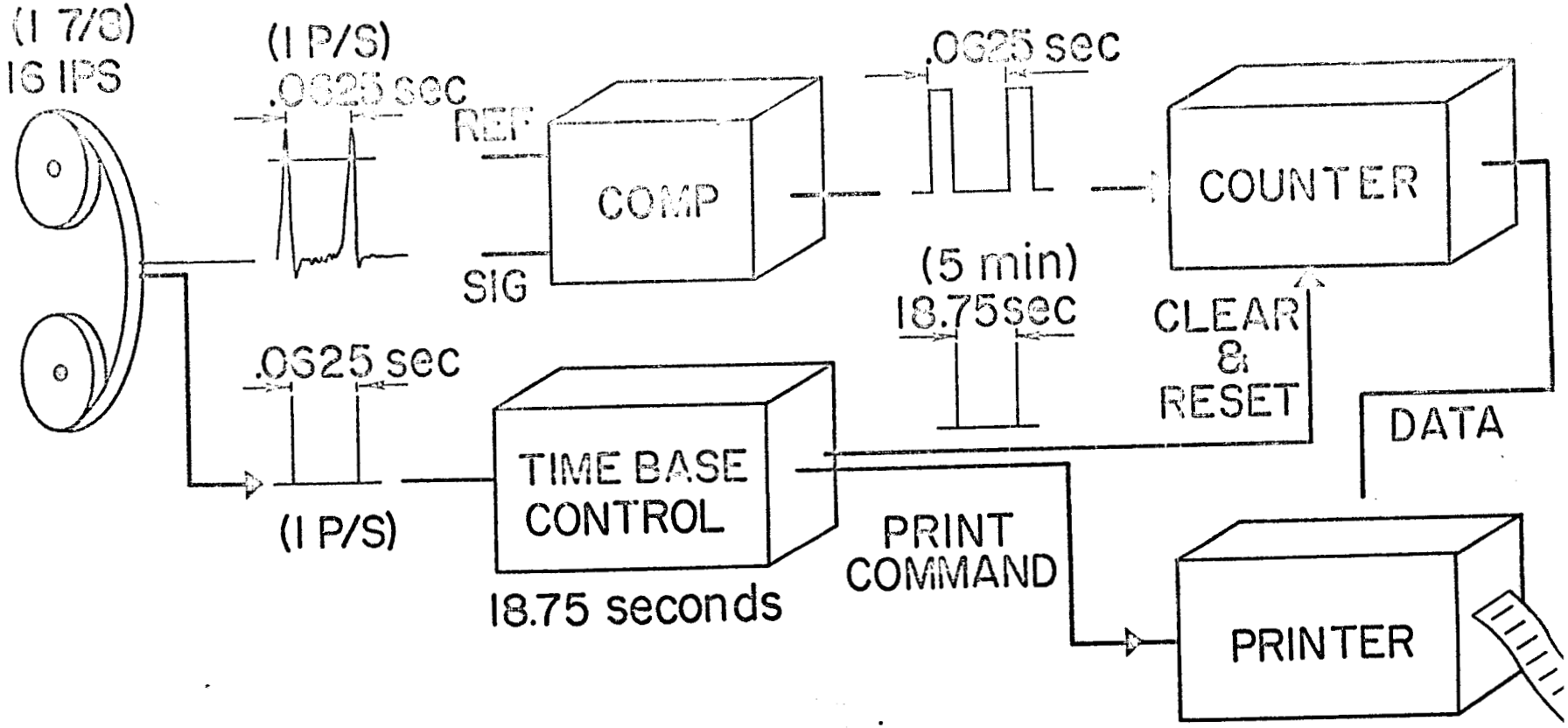
FIELD ENABLES
ELEMENT ENABLES

INDIVIDUAL ELEMENT CONTROLS

CONTROL ELEMENTS

Fig 11

BASIC METHOD OF COMPUTING AVERAGE HEART RATE FROM ECG RECORDS



	TAPE SPEED IPS	ECG RATE	AVERAGING INTERVAL	TOTAL RUNNING
RECORD TIMING	1 7/8	~1 P/S	5 min	7 DAYS
PLAYBACK TIMING	16	.0625	18.75 sec	10.5 hrs

READOUT = $\frac{\text{HEART BEATS}}{\text{5min}}$ →

Fig 12

NOISE DISCRIMINATION TECHNIQUE FOR RECURRENT OR PERIODIC DATA

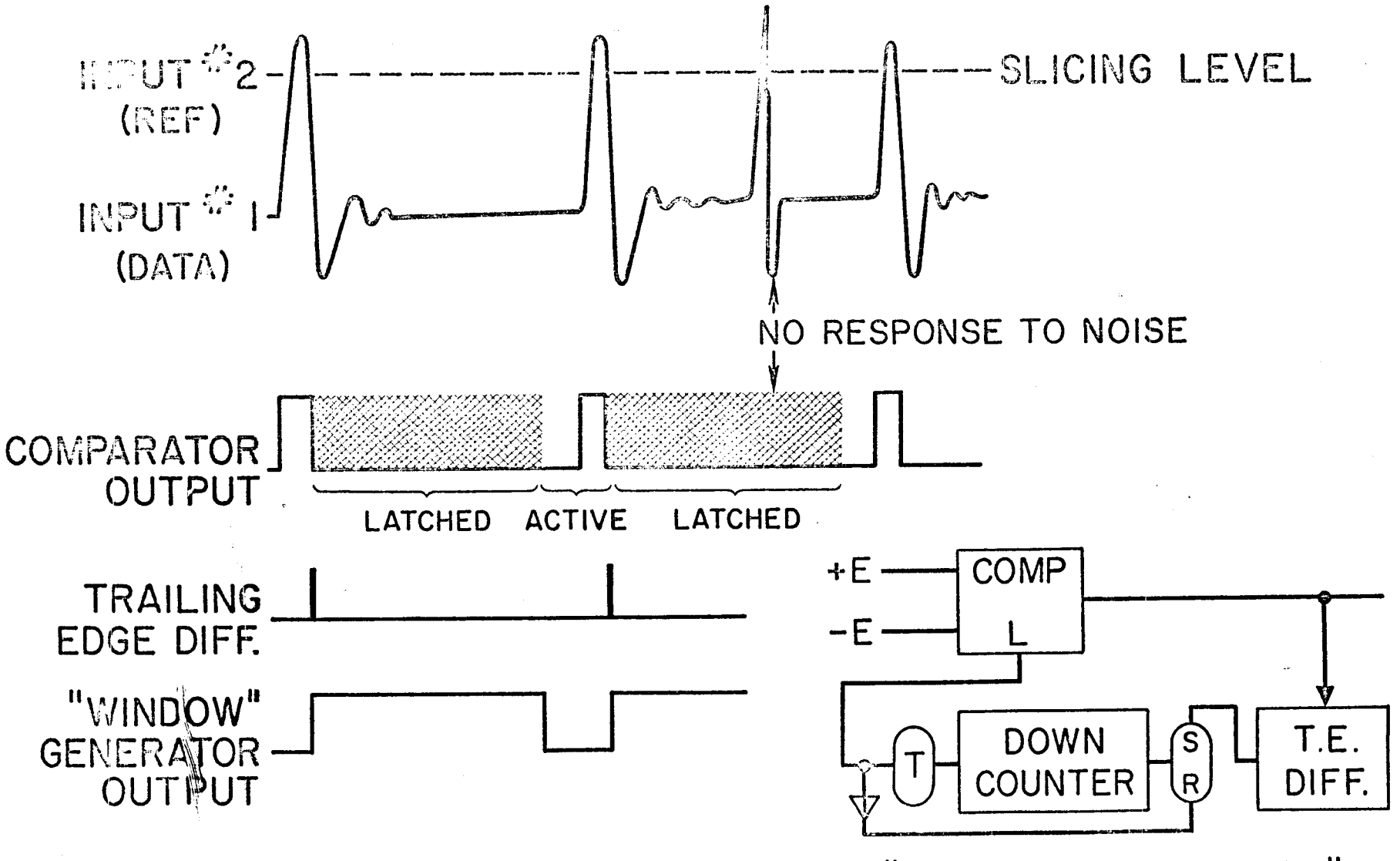
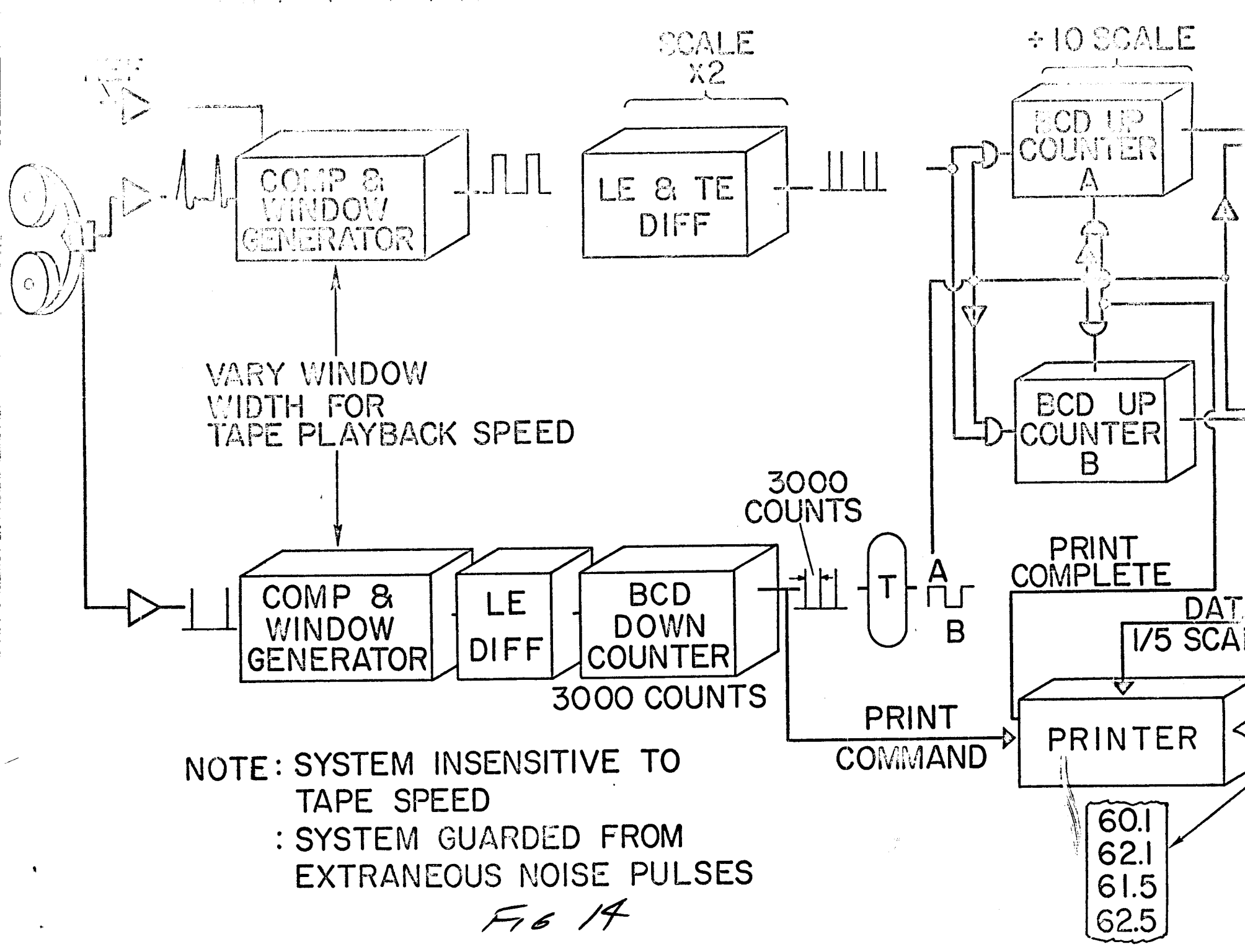


Fig 13



NOTE: SYSTEM INSENSITIVE TO TAPE SPEED
: SYSTEM GUARDED FROM EXTRANEOUS NOISE PULSES

Fig 14

A-30822

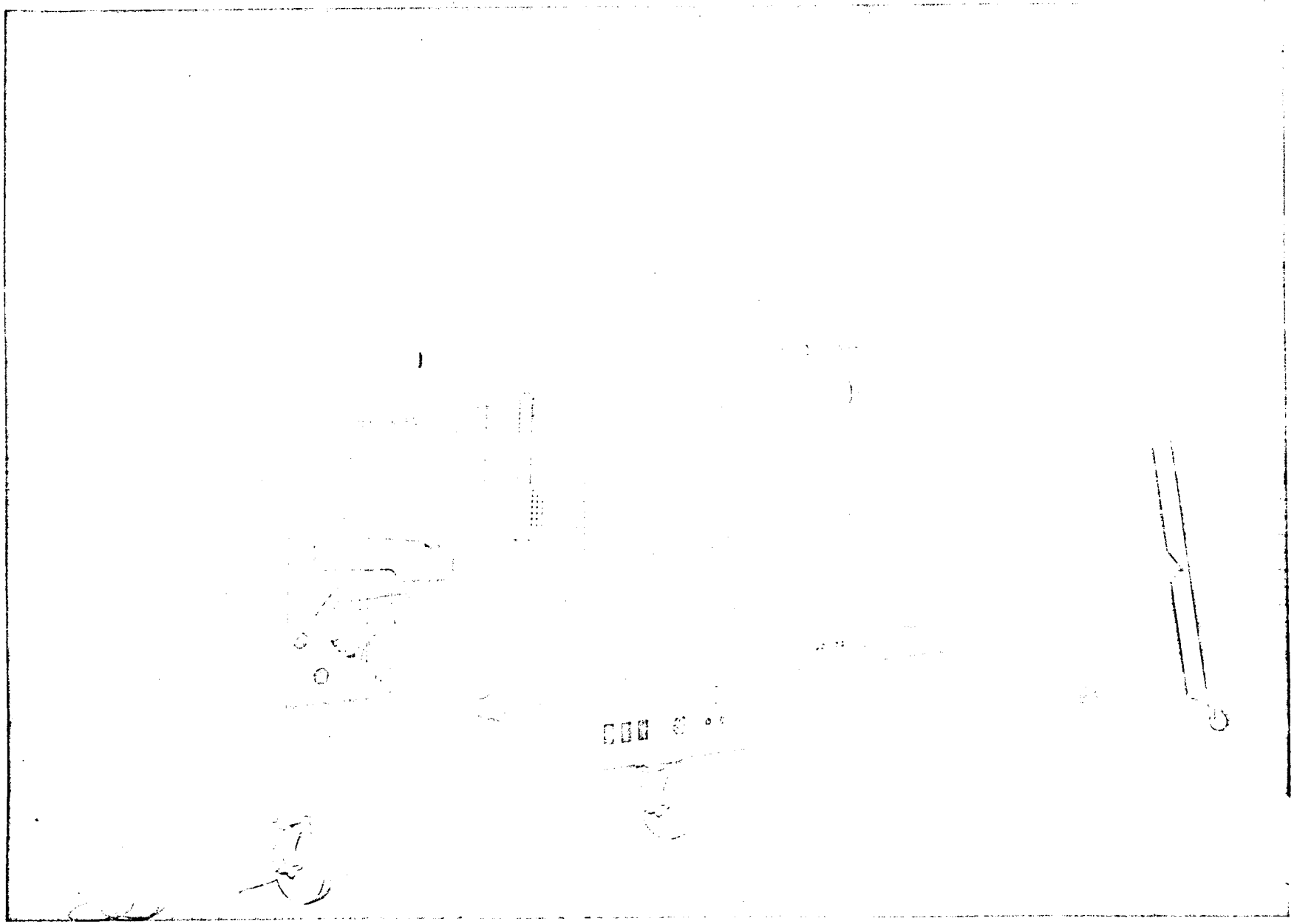


Fig 15

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
AMES RESEARCH CENTER, MOFFETT FIELD, CALIFORNIA

TRACKING TASK SIMULATOR SHOWING DLS FUNCTIONS

DLS COMPONENTS IN RED

ANALOG COMPONENTS IN BLACK

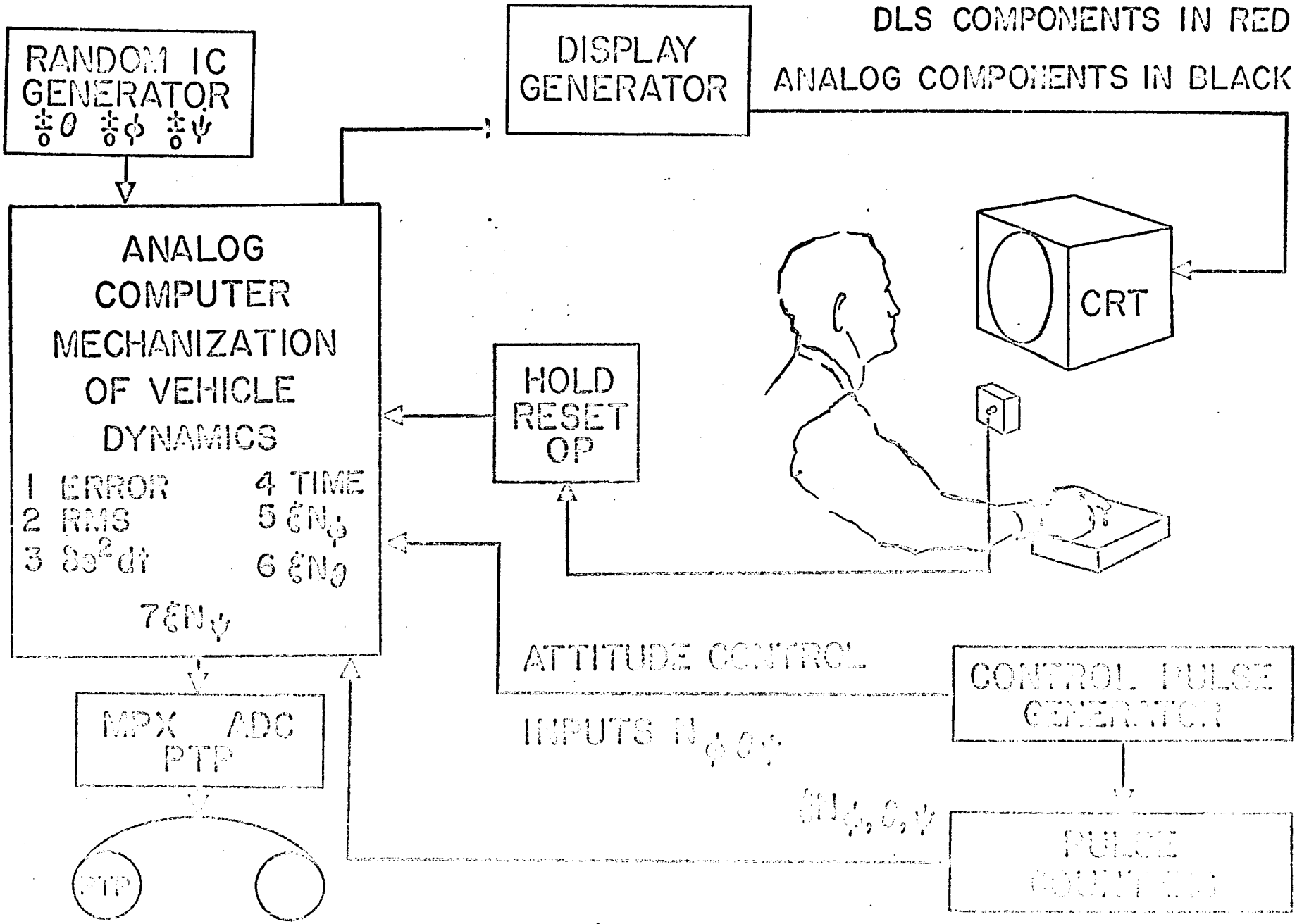


FIG 16

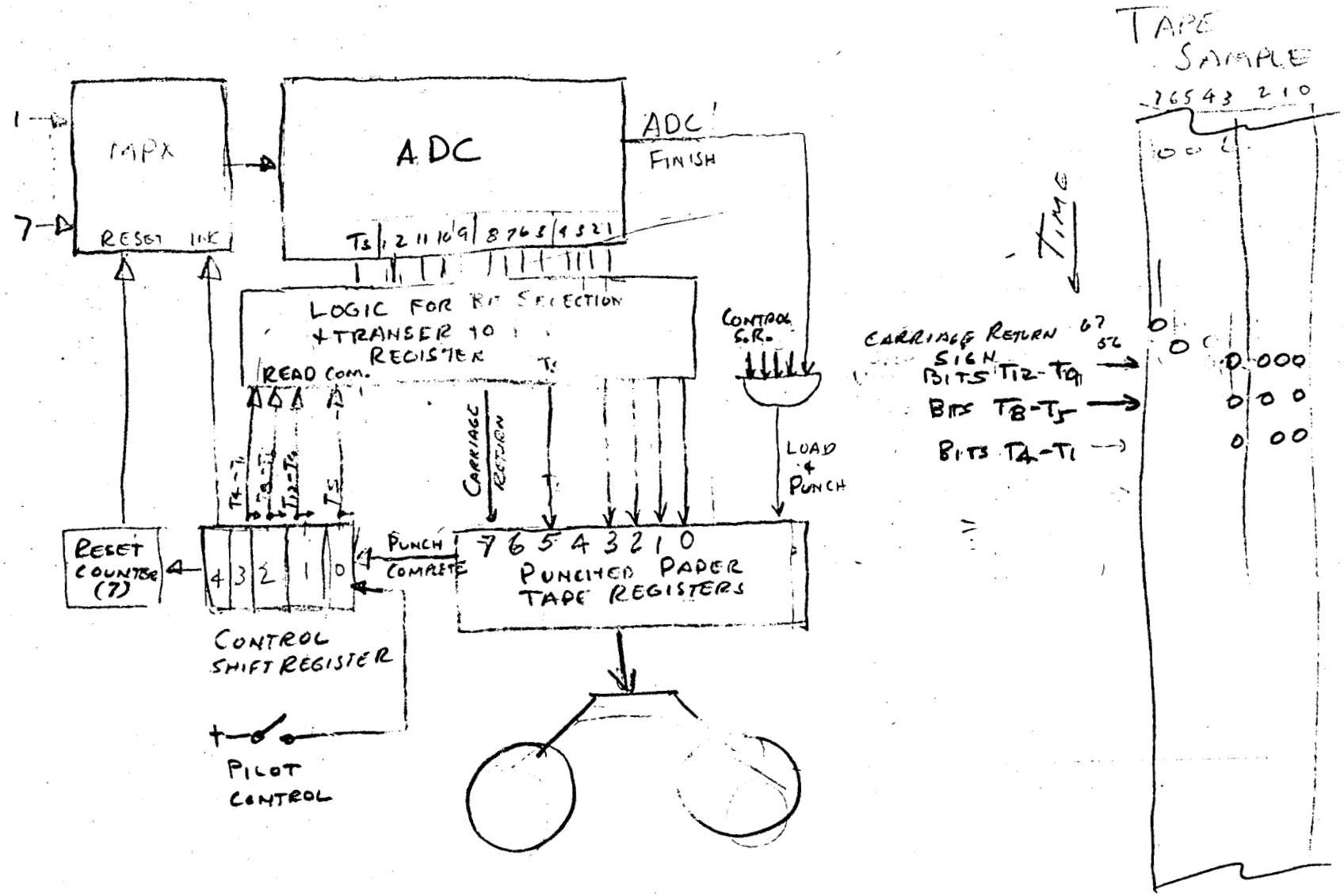


FIG (17) SIMPLIFIED DIAGRAM OF D.L.S. PROGRAM FOR OUTPUT OF ANALOG DATA + SAMPLE TAPE FORMAT

PROGRAM TO INTRODUCE TIME DELAYS IN ANALOG SIGNALS USING DLS TECHNIQUES

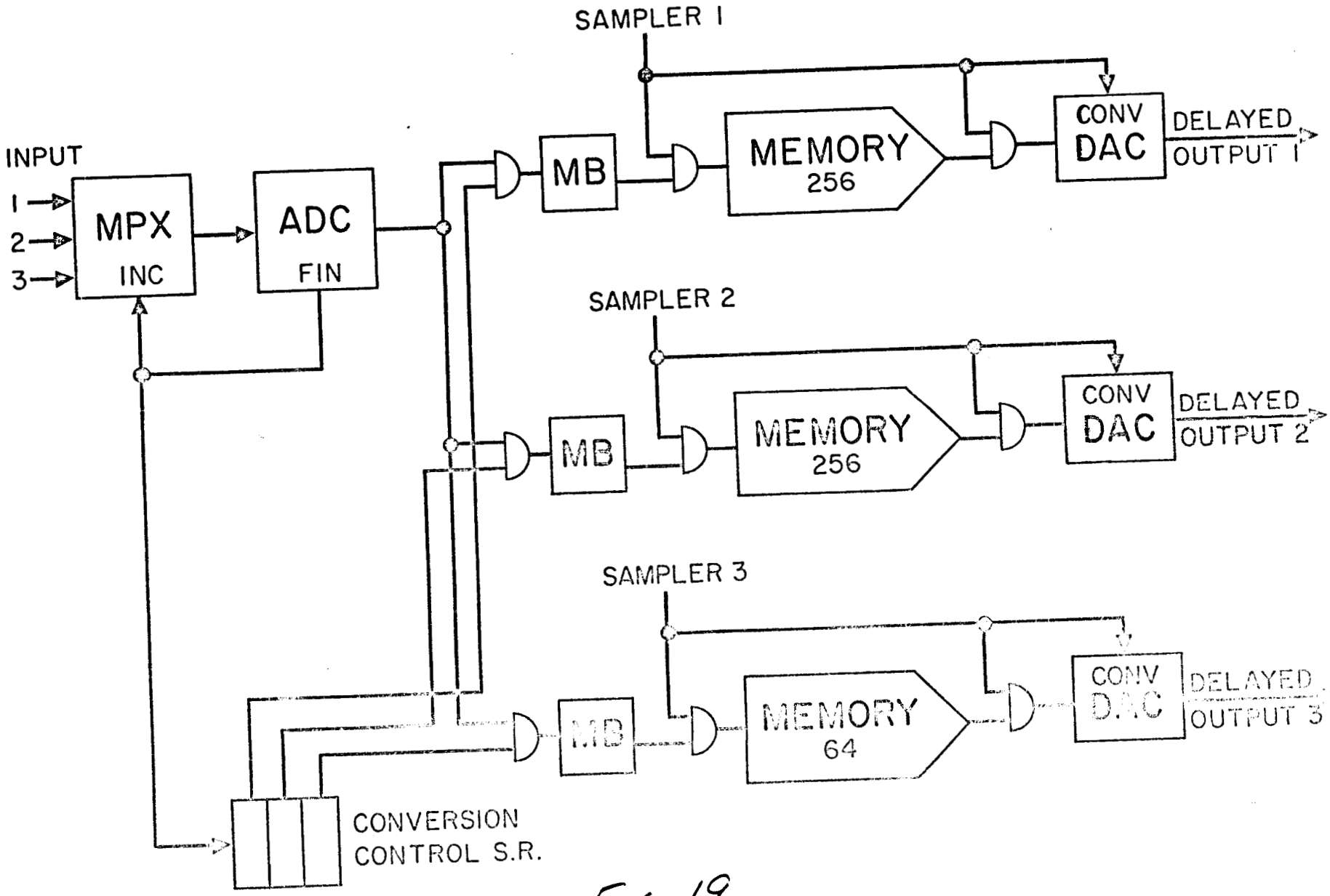


Fig 19